What is claimed is:

1. A test circuit for a second macro block that performs transmission and reception processing to and from a first macro block at a first clock frequency, the test circuit comprising:

a test transmission buffer which stores a transmission data signal from a test input terminal at a second clock frequency that is lower than the first clock frequency; and

a test reception buffer which outputs a reception data signal from the second macro block to a test output terminal at a third clock frequency that is lower than the first clock frequency,

wherein, after storing the transmission data signal from the test input terminal at the second clock frequency, the test transmission buffer outputs the stored transmission data signal to the second macro block at the first clock frequency, the second macro block including a physical-layer circuit for data communications, and

wherein, after storing the reception data signal from the second macro block at the first clock frequency, the test reception buffer outputs the stored reception data signal to the test output terminal at the third clock frequency.

2. The test circuit as defined in claim 1,

wherein, when the second macro block that has received the transmission data signal performs transmission and reception processing in a loopback mode over a first bus that differs from a bus between the first and second macro blocks, and has output the reception data signal received in loopback mode to the first macro block side at the first clock frequency,

the test reception buffer stores the reception data signal from the second macro block at the first clock frequency and outputs the stored reception data signal to the test

output terminal at the third clock frequency.

3. The test circuit as defined in claim 1, further comprising:

a communications sequencer for performing transmission and reception processing to and from the second macro block by a predetermined communications protocol,

wherein the communications sequencer performs processing for transmitting the transmission data signal stored in the test transmission buffer to the second macro block at the first clock frequency, and performs processing for receiving the reception data signal from the second macro block into the test reception buffer at the first clock frequency.

4. The test circuit as defined in claim 1, further comprising:

a first selector having a first input to which an output signal from the first macro block is input and a second input to which the transmission data signal from the test transmission buffer is input; and

a second selector having a first input to which an output signal from the first selector is input and a second input to which the reception data signal from the second macro block is input,

wherein, during a second test mode for testing the second macro block:

the first selector outputs the transmission data signal that has been input to the second input of the first selector to the second macro block; and

the second selector outputs the reception data signal from the second macro block that has been input to the second input of the second selector to the test reception buffer.

5. The test circuit as defined in claim 4,

wherein, during a first test mode for testing the first macro block:

the first selector outputs to the second selector the output signal from the first macro block that has been input to the first input of the first selector; and

the second selector outputs to the first macro block the output signal from the first selector that has been input to the first input of the second selector.

6. The test circuit as defined in claim 5,

wherein a scan path is set for the test circuit together with the first macro block, and

wherein the first test mode is a scan mode in which testing is performed by a scan method that uses the scan path.

7. The test circuit as defined in claim 6,

wherein, when the number of the output signals from the first macro block to the test circuit is I and the number of input signals from the test circuit to the first macro block is J (where I > J, I and J are integers greater than or equal to two), the test circuit comprises (I-J) dummy scan flip-flops which holds (I-J) output signals among the I output signals from the first selector, and

wherein the dummy scan flip-flops output the held output signals through the scan path in the scan mode.

8. An integrated circuit comprising:

the test circuit as define in claim 1;

the first macro block; and

the second macro block.

9. An integrated circuit comprising:

the test circuit as define in claim 2;

the first macro block; and

the second macro block.

10. An integrated circuit comprising:

the test circuit as define in claim 3;

the first macro block; and

the second macro block.

11. An integrated circuit comprising:

the test circuit as define in claim 4;

the first macro block; and

the second macro block.

12. An integrated circuit comprising:

the test circuit as define in claim 5;

the first macro block; and

the second macro block.

13. An integrated circuit comprising:

the test circuit as define in claim 6;

the first macro block; and

the second macro block.

14. An integrated circuit comprising:

the test circuit as define in claim 7;

the first macro block; and

the second macro block.

15. A test method for testing for a second macro block which performs transmission and reception processing to and from a first macro block at a first clock frequency, using a test circuit including a test transmission buffer and a test reception buffer, the test method comprising:

storing a transmission data signal from a test input terminal into the test transmission buffer at a second clock frequency that is lower than the first clock frequency and, after the transmission data signal has been stored, outputting the stored transmission data signal to the second macro block at the first clock frequency, the second macro block including a physical-layer circuit for data communications; and

storing a reception data signal from the second macro block into the test reception buffer at the first clock frequency and, after the reception data signal has been stored, outputting the stored reception data signal to the test output terminal at a third clock frequency that is lower than the first clock frequency.

16. The test method as defined in claim 15,

wherein, when the second macro block that has received the transmission data signal performs transmission and reception processing in loopback mode and has output the reception data signal received in loopback mode at the first clock frequency, the output reception data signal is stored in the test reception buffer at the first clock frequency and the stored reception data signal is output to the test output terminal at the third clock frequency.

17. The test method as defined in claim 15,

wherein the test circuit comprises a communications sequencer for performing transmission and reception processing to and from the second macro block by a

predetermined communications protocol,

wherein the communications sequencer is used for transmitting the transmission data signal, which has been stored in the test transmission buffer, to the second macro block at the first clock frequency, and

wherein the communications sequencer is used for receiving the reception data signal from the second macro block into the test reception buffer at the first clock frequency.

18. The test method as defined in claim 15,

wherein the test circuit comprises:

a first selector having a first input to which an output signal from the first macro block is input and a second input to which the transmission data signal from the test transmission buffer is input; and

a second selector having a first input to which an output signal from the first selector is input and a second input to which the reception data signal from the second macro block is input, and

wherein, during a second test mode for testing the second macro block:

a transmission data signal that has been input to the second input of the first selector is output to the second macro block; and

the reception data signal from the second macro block, which has been input to the second input of the second selector, is output to the test reception buffer.

19. The test method as defined in claim 18,

wherein, during a first test mode for testing the first macro block:

the output signal from the first macro block that is input to the first input of the first selector is output to the first input of the second selector; and

the output signal from the first selector that has been input to the first input of

the second selector is output to the first macro block.

20. The test method as defined in claim 19,

wherein a scan path is set for the test circuit together with the first macro block, and

wherein testing is performed in scan mode by a scan method that uses the scan path, in the first test mode.

21. The test method as defined in claim 20,

wherein, when the number of the output signals from the first macro block to the test circuit is I and the number of input signals from the test circuit to the first macro block is J (where I > J, I and J are integers greater than or equal to two), (I-J) output signals among the I output signals from the first selector are held in dummy scan flip-flops, and

wherein the held output signals are output through the scan path in the scan mode.